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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/572,730	03/21/2006	Hiroshi Oji	40404.30/tt	6903
54068	7590	07/10/2009		
ROHM CO., LTD. C/O KEATING & BENNETT, LLP 1800 Alexander Bell Drive SUITE 200 Reston, VA 20191			EXAMINER HUYNH, ANDY	
			ART UNIT 2818	PAPER NUMBER
			NOTIFICATION DATE 07/10/2009	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/572,730	Applicant(s) OJI, HIROSHI	
	Examiner ANDY HUYNH	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 March 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 2 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This is responsive to Applicant's Amendment filed March 31, 2009. In view of the Amendment, Claims **3-5** have been canceled is acknowledged. Currently, Claims **1 and 2** are pending in the application.

Response to Arguments

Applicant's arguments filed March 31, 2009, with respect to the rejections have been fully considered but they are not persuasive.

In response to Applicant's arguments that Mariko does not teach or suggest the features of "the low-concentration layer being formed in an extreme surface layer of a channel portion of the well" or "a n-type low-concentration layer being formed in an extreme surface layer of a channel portion of the n-type well" as recited in Claims **1 and 2**. Particularly, Mariko teaches that the portion of the high concentration p-type semiconductor region 8 that the low concentration p-type surface layer 7 is formed on does not include a channel portion. The Examiner respectfully disagrees. Fig. 1 of Mariko clearly discloses, among other things, "the low-concentration layer 7 being formed in an extreme surface layer of a channel portion of the well 8" and the portion of the high concentration p-type semiconductor region 8 that the low concentration p-type surface layer 7 is formed on does include a channel portion which is formed between source/drain regions 6 as recited in Claims **1 and 2**. Therefore, the Examiner believes that Mariko still reads on the claims. For the above reasons, it is believed that the rejections should be sustained. The rejections are re-provided as follows.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over JP03-276730, Applicant's submitted prior art (ASPA), in view of US 6,849,908 B2 to Hirano et al. hereinafter "Hirano."

JP03-276730 (ASPA) discloses in Fig. 1 a semiconductor device, comprising:

- a well 8 of a first conductive p⁺ type formed in an upper layer of a substrate 1;
- a low-concentration layer 7 of the first conductive p- type having a lower impurity concentration than the well 8, the low-concentration layer 7 being formed in an extreme surface layer of a channel portion of the well 8;
- a gate dielectric layer 2 formed on the low-concentration layer 7;
- a gate electrode 3 formed on the gate dielectric layer 2; and

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source/drain regions 6 of a second conductive n+ type formed in an upper layer of the well 8, the source/drain regions 6 sandwiching the low-concentration layer 7 (see English Abstract).

JP03-276730 does not explicitly disclose a gate dielectric layer being a high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film. Hirano teaches in Fig. 4 a similar semiconductor device comprising, inter alia, a high-k gate dielectric layer/a metal silicate layer 12a having a higher dielectric constant than a silicon oxide film to suppress leakage current flowing through the gate dielectric film (col. 1, lines 33-41, lines 49-50, and col. 5, line 62-col. 6, line 26). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a high-k gate dielectric layer/a metal silicate layer served as a gate dielectric film having a higher dielectric constant than a silicon oxide film, as taught by Hirano in the semiconductor device as disclosed by JP03-276730 in order to suppress leakage current flowing through the gate dielectric film (see Hirano, col. 6, lines 24-26).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 7,087,969 B2 to Nishiyama et al. hereinafter "Nishiyama" in view of JP03-276730, Applicant's submitted prior art (ASPA).

Nishiyama discloses in Fig. 1 and related texts as set forth in col. 4, line 45-col. 5, line 30, a complementary semiconductor device having a n-type circuit region 3 and a p-type circuit region 5, comprising:

a p-type well 9 formed in an upper layer of a substrate 1 of the n-type circuit region 3;

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a n-type well 19 formed in an upper layer of the substrate 1 of the p-type circuit region 5;
a high-k gate dielectric layer 13 made of hafnium silicate (HfSiON) including boron (B) formed on the p-type well 9 and a high-k gate dielectric layer 23 made of hafnium silicate (HfSiON) not substantially including boron (B) formed on the n-type well 19, it is inhering that the high-k gate dielectric layers 13/23 made of hafnium silicate (HfSiON) including boron (B)/hafnium silicate (HfSiON) not substantially including boron (B) having a higher dielectric constant than a silicon oxide film;

a gate electrode 15/25 formed on the high-k gate dielectric layer 13/23;

n-type source/drain regions 11 formed in an upper layer of the p-type well 9; and

p-type source/drain regions 21 formed in an upper layer of the n-type well 19.

Nishiyama does not explicitly disclose a p-type low-concentration layer formed in an extreme surface layer of a channel portion of the p-type well, the p-type low-concentration layer having a lower impurity concentration than the p-type well, a n-type low-concentration layer formed in an extreme surface layer of a channel portion of the n-type well, the n-type low-concentration having a lower impurity concentration than the n-type well, the n-type source/drain regions sandwiching the p-type low-concentration layer, and the p-type source/drain regions sandwiching the n-type low-concentration layer. JP03-276730 (ASPA) discloses in Fig. 1 a semiconductor device, comprising: a well 8 of a first conductive p⁺ type formed in an upper layer of a substrate 1; a low-concentration layer 7 of the first conductive p-type having a lower impurity concentration than the well 8, the low-concentration layer 7 being formed in an extreme surface layer of a channel portion of the well 8; a gate dielectric layer 2 formed on the low-concentration layer 7; a gate electrode 3 formed on the gate dielectric layer 2; and source/drain

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regions 6 of a second conductive n+ type formed in an upper layer of the well 8, the source/drain regions 6 sandwiching the low-concentration layer 7 (see English Abstract). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide a low-concentration layer formed in an extreme surface layer of a channel portion of the well having a lower impurity concentration than the well, as taught by JP03-276730 in the semiconductor device as disclosed by Nishiyama to arrive the claimed limitations, a p-type low-concentration layer formed in an extreme surface layer of a channel portion of the p-type well, the p-type low-concentration layer having a lower impurity concentration than the p-type well, a n-type low-concentration layer formed in an extreme surface layer of a channel portion of the n-type well, the n-type low-concentration having a lower impurity concentration than the n-type well, the n-type source/drain regions sandwiching the p-type low-concentration layer, and the p-type source/drain regions sandwiching the n-type low-concentration layer in order to decrease a threshold voltage and to suppress a short-channel effect (see JP03-276730, English Abstract).

Conclusion

THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

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CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh whose telephone number is (571) 272-1781. The examiner can normally be reached on Monday-Friday 6:30am-3:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

/Andy Huynh/

Primary Examiner, Art Unit 2818